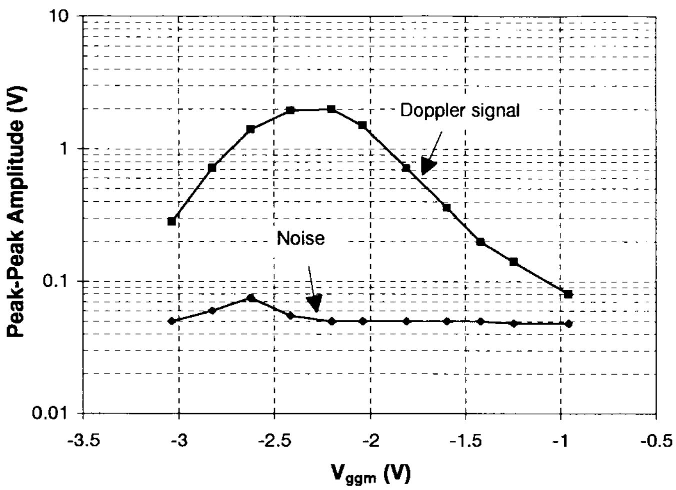

Fig. 4. Signal and noise output as a function of the bias voltage of the mixer.

sensitivity of the self-oscillating mixer scheme was about 27 dB worse than that of the optimum biased Doppler-radar transceiver front end. This is because of the high $1/f$ noise and shot noise of the oscillator FET. In the integrated Doppler-radar transceiver front-end design, the mixer FET operates at the origin of its I–V characteristics does not produce $1/f$ or shot noise [16]. Therefore, the overall system performance is greatly improved and independent of the used semiconductor devices.

IV. Conclusions

An integrated low-power Doppler-radar transceiver front end was developed using two adjacently spaced low-power FET active antennas, with one of them being biased to oscillate as the transmitter and the other being biased not to oscillate, but to act as the mixer. Operation theory was discussed and experimentally verified. This design demonstrated higher sensitivity at low Doppler frequencies than the self-oscillating mixer scheme. It can be used as the front end in low-power Doppler-radar systems such as intruder detectors.

Acknowledgment

The authors would like to thank L. Fan for etching the circuits.

References

[1] K. A. Hummer and K. Chang, "Spatial power combining using active microstrip patch antennas," *Microwave Opt. Technol. Lett.,* vol. 1, no. 1, pp. 8–9, Mar. 1988.
[2] J. A. Navarro, L. Fan, and K. Chang, "Active inverted stripline circular patch antennas for spatial power combining," *IEEE Trans. Microwave Theory Tech.,* vol. 41, pp. 1856–1863, Oct. 1993.
[3] ——, "Novel FET integrated inverted stripline patch," *Electron. Lett.,* vol. 30, no. 8, pp. 655–657, Apr. 14, 1994.
[4] B. K. Kormanyos and W. Harokopus, Jr., "CPW-fed active slot antennas," *IEEE Trans. Microwave Theory Tech.,* vol. 42, pp. 541–545, Apr. 1994.
[5] X. D. Wu and K. Chang, "Dual FET active patch elements for spatial power combiners," *IEEE Trans. Microwave Theory Tech.,* vol. 43, pp. 26–30, Jan. 1995.
[6] Z. Ding, L. Fan, and K. Chang, "A new type of active antenna for coupled Gunn oscillator driven spatial power combining arrays," *IEEE Microwave Guided Wave Lett.,* vol. 5, pp. 264–266, Aug. 1995.
[7] S. K. Masarweh, T. N. Sherer, K. S. Yngvesson, R. L. Gingras, C. Drubin, A. G. Cardiasmenos, and J. Wolverton, "Modeling of a monolithic slot ring quasi-optical mixer," *IEEE Trans. Microwave Theory Tech.,* vol. 42, pp. 1602–1609, Sept. 1994.
[8] K. Cha, S. Kawasaki, and T. Itoh, "Transponder using self-oscillating mixer and active antenna," in *IEEE MTT-S Int. Microwave Symp. Dig.,* San Diego, CA, May 23–27, 1994, pp. 425–428.
[9] R. Flynt, L. Fan, J. Navarro, and K. Chang, "Low cost and compact active integrated antenna transceiver for system applications," in *IEEE MTT-S Int. Microwave Symp. Dig.,* Orlando, FL, May 14–19, 1995, pp. 953–956.
[10] K. Kurokawa, "Some basic characteristics of broadband negative resistance oscillator circuits," *Bell Syst. Tech. J.,* vol. 48, pp. 1937–1955, July–Aug. 1969.
[11] K. Chang, *Microwave Solid-State Circuits and Applications.* New York: Wiley, 1994.
[12] Hewlett-Packard, *Communications Components Designer's Catalog, GaAs and Silicon Products.* Santa Rosa, CA: Hewlett-Packard Company, pp. 7, 69–70, 1993.
[13] B. A. Balanis, *Antenna Theory.* New York: Wiley, 1982.
[14] K. Chang, K. A. Hummer, and J. L. Klein, "Experiments on injection locking of active antenna elements for active phased arrays and spatial power combiners," *IEEE Trans. Microwave Theory Tech.,* vol. 37, pp. 1078–1084, July 1989.
[15] G. T. Ruck, *Radar Cross Section Handbook.* New York: Plenum, 1970.
[16] K. Laker and W. Sansen, *Design of Analog Integrated Circuits and Systems.* New York: McGraw-Hill, 1994.

60-GHz Monolithic Down- and Up-Converters Utilizing a Source-Injection Concept

Mohammad Madihian, Laurent Desclos, Kenichi Maruhashi, Kazuhiko Onda, and Masaaki Kuzuhara

***Abstract*—This paper deals with the design considerations, fabrication process, and performance of coplanar waveguide (CPW) heterojunction FET (HJFET) down- and up-converter monolithic microwave integrated circuits (MMIC's) for V-band wireless system applications. To realize a mixer featuring a simple structure with inherently isolated ports, and yet permitting independent port matching and low local oscillator (LO) power operation, a "source-injection" concept is utilized by treating the HJFET as a three-port device in which the LO signal is injected through the source terminal, the RF (or IF) signal through the gate terminal, and the IF (or RF) signal is extracted from the drain terminal. The down-converter chip incorporates an image-rejection filter and a source-injection mixer. The up-converter chip incorporates a source-injection mixer and an output RF filter. With an LO power and frequency of 7 dBm and 60.4 GHz, both converters can operate at any IF frequency within 0.5–2 GHz, with a corresponding conversion gain within -7 to -12 dB, primarily dominated by the related filter's insertion loss. Chip size is 3.3 mm$\times$2 mm for the down-converter, and 3.5 mm $\times$ 1.8 mm for the up-converter.**

I. Introduction

Recent advances in wireless services have motivated development of low-cost small-size frequency-converter modules with 1–2 GHz IF

Manuscript received February 10, 1997; revised April 7, 1998.
M. Madihian and L. Desclos are with the Wireless Network Technology Group, C&C Media Research Laboratories, NEC Corporation, Kawasaki 216, Japan.
K. Maruhashi, K. Onda, and M. Kuzuhara are with the Kansai Electronics Research Laboratory, NEC Corporation, Shiga 520, Japan.
Publisher Item Identifier S 0018-9480(98)04939-4.

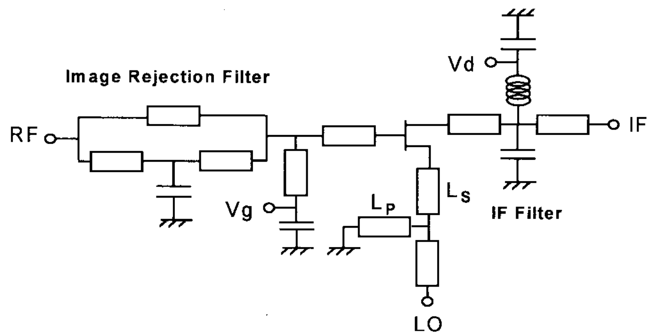

Fig. 1. V-band down-converter equivalent circuit.

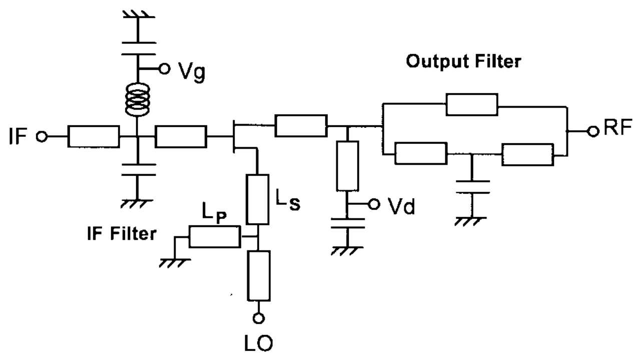

Fig. 2. V-band up-converter equivalent circuit.

frequencies for facilitating 100–200 Mb/s transmission of data, voice, and video in a millimeter-wave wireless local area network (LAN) system. Mixers are key elements in a frequency converter, and require rigorous design methods to achieve optimum operation. It is desirable to develop mixers featuring a simple structure with inherently isolated ports, and yet, permitting independent port matching and low local oscillator (LO) power operation.

Conventional FET mixers employ either a "gate mixing" or a "drain injection" topology to produce the desired frequency component by applying the LO signal to the gate or drain terminals of the device, respectively [1]–[8]. Introducing a "source-injection" concept, and treating an FET as a "three-port device," we have recently proposed a class of FET mixers with the above features, which has been confirmed for a 24-GHz up-converter [9]. This paper applies the same circuit topology to develop a 60-GHz down-converter as well as an up-converter by redesigning the frequency selective elements such as filters and quarter-wavelength transmission lines in the converter circuits accordingly.

II. Circuit Design

Equivalent circuits for the coplanar waveguide (CPW) V-band down-converter and up-converter monolithic microwave integrated circuits (MMIC's) are shown in Figs. 1 and 2, respectively.

A. Down-Converter

The down-converter comprises an RF image-rejection filter and a source-injection down-mixer utilizing a heterojunction FET (HJFET) as a mixing element. The RF signal, after passing through the image-rejection filter and RF matching network, is applied to the HJFET gate terminal. The LO signal is applied to the HJFET source terminal through the LO matching network. The resultant IF signal is extracted from the HJFET drain terminal after passing through the IF matching network. From Fig. 1, the RF image-rejection filter consists of two T-type networks connected in parallel for suppressing both the image and LO frequencies. Use is made of spiral inductors in the IF matching network for resonant-type filtering and IF frequency matching. The LO matching network allows unconditionally stable operation for the down-converter, both in the presence and absence of an LO signal. The short-circuited transmission line L_P in the LO matching network facilitates the transistor's gate and drain dc biasing.

B. Up-Converter

The up-converter comprises a source-injection up-mixer and an output filter to suppress the LO signal and other unwanted frequencies. The IF signal, after passing through the IF matching network, is applied to the HJFET gate terminal, and the LO signal is applied to the HJFET source terminal through the LO matching network. The resultant RF signal is extracted from the HJFET drain terminal after passing through the RF matching network and the filter which consists of two T-type networks connected in parallel. Similarly, use is made of spiral inductors in the IF matching network for resonant-type filtering and IF frequency matching. The LO matching network for the up-converter is the same as the one for the down-converter MMIC.

The structures described utilize the inherent isolation characteristics of the FET terminals under the pinch off condition to separate the IF, LO, and RF signals without the use of any hybrid circuit. Since the LO signal is directly applied to the source terminal, the LO has the largest effect on the device transconductance modulation and, consequently, on nonlinear mixing enhancement, facilitating a low LO power operation.

Both small-signal linear and large-signal nonlinear parameters of a discrete 0.15 μm$\times$ 100 μm AlGaAs/InGaAs HJFET were used in the circuit design. To investigate the stability of each mixer, the three-port network was reduced to a two-port network by replacing the LO source with a 50-Ω termination, and stability factor K and the stability measure $B1$ were simulated by sweeping the drain current, which represents the effect of the LO signal on FET transconductance modulation. Unconditional stability of the converters was assured by optimizing the series transmission line L_S in the LO matching network. Details of the circuit design steps are discussed in [13].

III. Fabrication Process and Device Characteristics

The V-band down- and up-converter MMIC's were fabricated on a 3-in undoped Si GaAs substrate. Molecular beam epitaxy (MBE) AlGaAs/InGaAs HJFET's were used in the MMIC's. A CPW structure was used for transmission lines which permits chip-size reduction and realization of transmission lines with different characteristic impedances without affecting the overall chip layout. To suppress odd modes, metal bridges were extensively employed to connect ground planes along the lines, particularly in the vicinity of a line discontinuity. A metal–insulator–metal (MIM) structure was applied for fabricating dc blocking and bypass capacitors. The HJFET used in the converter MMIC's has a gate length of 0.15 μm and a total gatewidth of 100 μm (50 μm$\times$ 2 fingers). Typical transconductance of 380 mS/mm and f_T of 70 GHz, both at a drain bias of 4 V, and a reverse gate–drain breakdown voltage of 10 V have been measured for the HJFET's. Measured pinchoff voltage for the HJFET is -1.6 V.

IV. Performance

On-wafer Cascade Microtech probes were utilized to evaluate the chip performance.

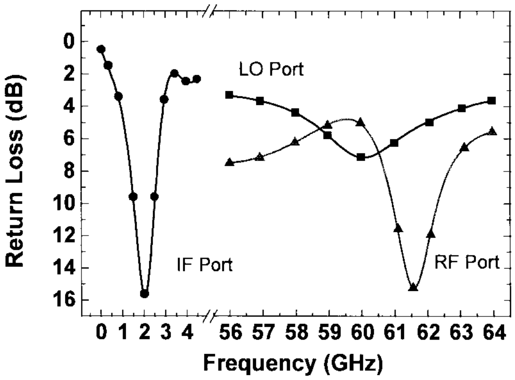

Fig. 3. Down-converter small-signal matching characteristics for RF, LO, and IF ports.

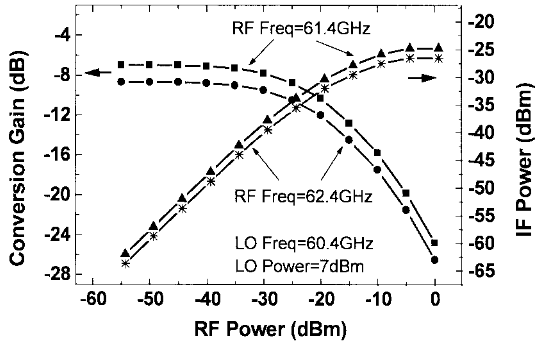

Fig. 4. Down-converter conversion gain and IF output power versus RF power.

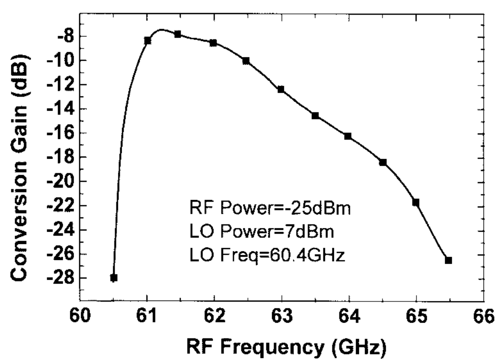

Fig. 5. Down-converter conversion gain versus RF frequency.

A. Down-Converter

The complete V-band CPW down-converter integrated circuit (IC) has a chip size of 3.3 mm$\times$ 2 mm. The FET gate bias was -1.6 V, corresponding to the pinchoff voltage, and the drain bias was 0.7 V. Fig. 3 shows small-signal matching characteristics for the IF, LO, and RF ports. Measured in-band return loss for the IF and RF ports is better than 15 dB, and for the LO port is better than 8 dB. LO suppression at the RF and IF ports is better than 22 dB, and RF suppression at the IF port is better than 25 dB. Measured passband and rejection-band insertion loss for the image-rejection filter were 7 and 16 dB, respectively.

Large-signal down-converter measurement results are shown in Figs. 4–6. Fig. 4 depicts conversion gain as well as IF output power variation versus RF power at 61.4 and 62.4 GHz for an LO power and frequency of 7 dBm and 60.4 GHz. Conversion gain is constant for RF power levels lower than -35 dBm. Fig. 5 represents conversion gain versus RF frequency for an RF power of -25 dBm and an LO power of 7 dBm at 60.4 GHz. The down-converter has an

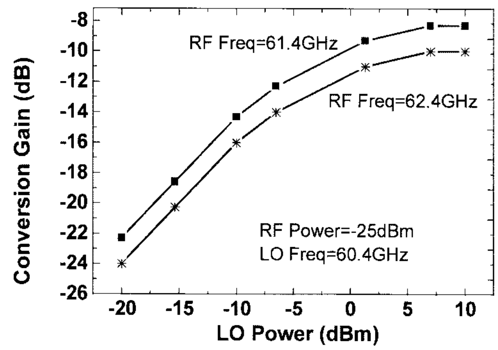

Fig. 6. Down-converter conversion gain versus LO power.

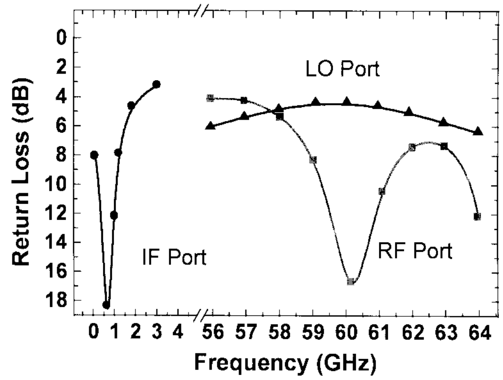

Fig. 7. Up-converter small-signal matching characteristics for RF, LO, and IF ports.

almost constant conversion gain for an RF frequency within the 60–62.5 GHz band. Fig. 6 exhibits conversion gain against LO power for an LO frequency of 60.4 GHz and an RF power of -25 dBm at 61.4 and 62.4 GHz. Conversion gain saturates for LO power levels higher than 7 dBm. As stated earlier, the conversion gain of the down-converter is dominated by the insertion loss of the image-rejection filter.

B. Up-Converter

The complete V-band CPW up-converter IC has a chip size of 3.5 mm $\times$ 1.8 mm. Fig. 7 shows small-signal matching characteristics for the IF, LO, and RF ports. Measured in-band return loss for the IF and RF ports is 8 dB, and for the LO port is 5 dB. LO suppression at the RF and IF ports is better than 20 dB, and RF suppression at the IF port is better than 47 dB.

Large-signal up-converter measurement results are shown in Figs. 8–10. Fig. 8 depicts conversion gain as well as IF output power variation versus IF power at 1 and 2 GHz for an LO power and frequency of 7 dBm and 60.4 GHz. Conversion gain is constant for IF power levels lower than -6 dBm. Fig. 9 represents conversion gain versus IF frequency for an IF power of -6 dBm and an LO power of 7 dBm at 60.4 GHz. Maximum conversion gain for the up-converter is -9 dB for an IF frequency of 1 GHz, which is dominated by the insertion loss of the output filter, as stated earlier. Fig. 10 exhibits conversion gain against LO power for an LO frequency of 60.4 GHz and an IF power of -6 dBm at 1 and 2 GHz.

V. Conclusions

Design consideration and performance results for CPW down-converter as well as up-converter MMIC's incorporating source-injection mixers and RF filters were described. In the circuit design, the FET was treated as a three-port device in which the LO signal is

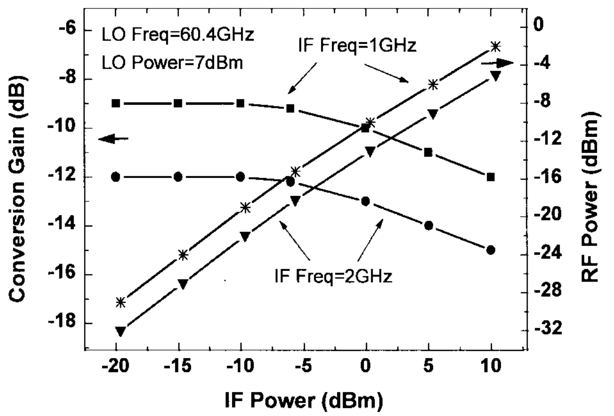

Fig. 8. Up-converter conversion gain and RF output power versus IF power.

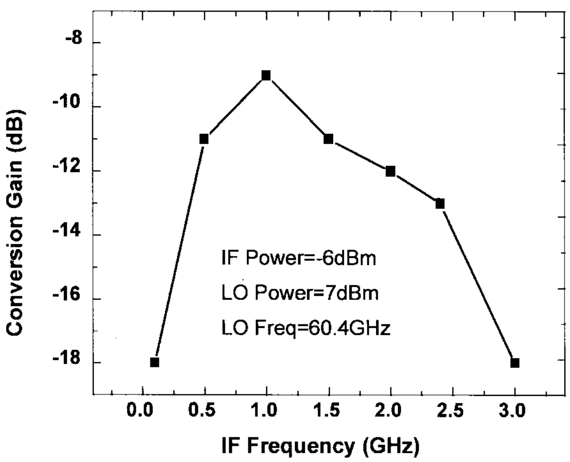

Fig. 9. Up-converter conversion gain versus IF frequency.

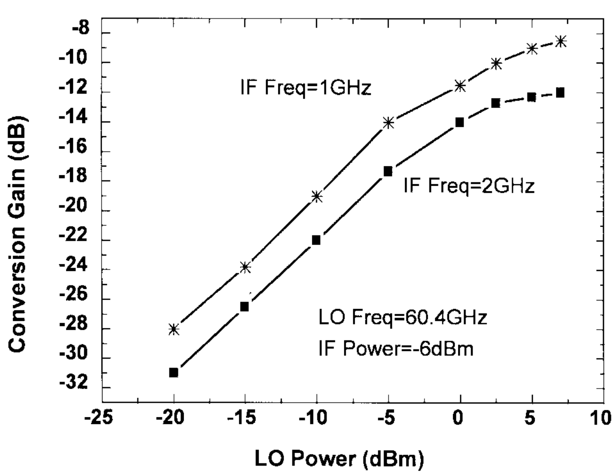

Fig. 10. Up-converter conversion gain versus LO power.

applied to the source terminal. With an LO power and frequency of 7 dBm and 60.4 GHz, both converters can operate at any IF frequency within 0.5–2 GHz, with a corresponding conversion gain within -7 to -12 dB, which is primarily dominated by the related filter's insertion loss. The frequency converters reported in this paper are expected to find applications in millimeter-wave wireless LAN systems.

REFERENCES

[1] R. A. Pucel, D. Masse, and R. Bera, "Performance of GaAs MESFET mixers at X-band," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-24, pp. 351–360, June 1976.

[2] C. C. Penalosa and C. Aichison, "Analysis and design of MESFET gate mixer," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-35, pp. 643–652, July 1987.

[3] P. Bura and R. Dikshit, "FET mixer with the drain LO injection," *Electron. Lett.*, vol. 12, no. 20, pp. 536–537, Sept. 1976.

[4] G. Tomassetti, "An unusual microwave mixer," in *Proc. European Microwave Conf.*, Dublin, Ireland, Sept. 1986, pp. 754–757.

[5] V. Brady, T. Hsu, R. Reeves, and M. Vermeulen, "Development of a monolithic FET Ka-band single side band up-converter and image reject down-converter," in *IEEE GaAs IC Symp. Dig.*, San Diego, CA, Oct. 1989, pp. 189–192.

[6] W. R. Brinlee, A. M. Pavio, C. L. Goldsmith, and W. J. Thompson, "A monolithic multifunction EW broad-band receiver converter," in *IEEE GaAs IC Symp. Dig.*, San Jose, CA, Oct. 1993, pp. 207–210.

[7] T. Hirota and M. Muraguchi, "K-band frequency up-converters using reduced-size couplers and dividers," in *IEEE GaAs IC Symp. Dig.*, Monterey, CA, Oct. 1991, pp. 53–56.

[8] A. Minakawa and T. Hirota, "An extremely small 26-GHz monolithic image-rejection mixer without DC power consumption," *IEEE Trans. Microwave Theory Tech.*, vol. 41, p. 1634–1637, Sept. 1993.

[9] M. Madihian, L. Desclos, K. Muruhashi, K. Onda, and M. Kuzuhara, "A monolithic AlGaAs/InGaAs up-converter IC for K-band wireless networks," *IEEE Trans. Microwave Theory Tech.*, vol. 43, pp. 2773–2778, Dec. 1995.

Physical Scaling Rules for AlGaAs/GaAs Power HBT's Based on a Small-Signal Equivalent Circuit

U. Schaper and P. Zwicknagl

***Abstract*—Physical scaling rules for AlGaAs/GaAs heterojunction bipolar transistors (HBT's) containing 2–16 emitter fingers are demonstrated. The parameter extraction is based on a small-signal equivalent circuit. The scaling parameters compare favorably with the measured data from the process control monitor.**

***Index Terms*—Heterojunction bipolar transistor, parameter extraction, scaling rules, small-signal model.**

I. INTRODUCTION

GaAs-based heterojunction bipolar transistors (HBT's) are promising power devices for L-band (mobile telephone) and X-band (radar) applications. Based on a T-shaped small-signal equivalent circuit, scaling rules for multifinger power HBT's have been derived to allow for the optimization of multiemitter cell design and monolithic microwave integrated circuits (MMIC's). Each circuit element is assigned a physical property by comparison with the equivalent circuit of the HBT topology. The derived physical scaling rules hold not only for various emitter areas [1], but also for all critical device design parameters. As a result, the rules can be used to evaluate multifinger unit cells [2] and provide feedback for process control data.

Manuscript received February 27, 1997; revised April 7, 1998.
The authors are with Siemens AG, Corporate Technology, Department ZT KM 5, D-81730 Munich, Germany (e-mail: ulrich.schaper@mchp.siemens.de).
Publisher Item Identifier S 0018-9480(98)04947-3.